[What is claimed is:]

1. A data interpolating device, comprising:

plural stages of delay circuits for successively delaying discrete data sequentially inputted; and

a multiplication/addition circuit that performs weighted addition of data outputted from the output stages of said plural stages of delay circuits according to the value of a digital basic function and thereby determines interpolation data for said discrete data sequentially inputted.

2. The data interpolating device according to claim 1,

a plurality of over-sampling circuits are cascade connected, when one set of over-sampling circuit comprises said plural stages of delay circuits and said multiplication/addition circuit.

3. A data interpolating device, comprising:

three stages of delay circuits for successively delaying discrete data sequentially inputted; and

a multiplication/addition circuit that performs weighted addition of data outputted from the output stages of said three stages of delay circuits according to the value of a digital basic function and thereby determines interpolation data for said discrete data sequentially inputted.

4. The data interpolating device according to claim 3,

said multiplication/addition circuit comprising:

a first multiplication unit for multiplying the output data of a first stage delay circuit by -1;

a second multiplication unit for multiplying the output data of a second stage delay circuit by 8;

a third multiplication unit for multiplying the output data of a third stage delay circuit by -1;

a first switching circuit for selectively switching between the output data of said first stage delay circuit and the output data of said first multiplication unit;

a second switching circuit for selectively switching between the output data of said third stage delay circuit and the output data of said third multiplication unit; and

an adder for adding the output data of said second multiplication unit, the output data of said first switching circuit and the output data of said second switching circuit.

5. The data interpolating device according to claim 3, said multiplication/addition circuit comprising:

a first multiplication/addition circuit composed of a first multiplication unit for multiplying the output data of the first stage delay circuit by -1, a second multiplication unit for multiplying the output data of the second stage delay circuit by 8, and an adder for adding the output data of said first multiplication unit, the output data of said second multiplication unit, and the output data of the third stage delay circuit;

a second multiplication/addition circuit composed of a third multiplication unit for multiplying the output data of the second stage delay circuit by 8, a fourth multiplication unit for multiplying the output data of the third stage delay circuit by -1, and an adder for adding the output data of said third multiplication unit, the output data of said fourth multiplication unit, and the output data of said first stage delay circuit; and

a switching circuit for selectively switching between the output data of said first multiplication/addition circuit and the output data of said second multiplication/addition circuit.

6. The data interpolating device according to claim 3, said multiplication/addition circuit comprising:

a first multiplication unit for multiplying the output data of the first stage delay circuit by -1;

a second multiplication unit for multiplying the output data of the second stage delay circuit by 8;

a third multiplication unit for multiplying the output data of the third stage delay circuit by -1;

a first adder for adding the output data of said first multiplication unit, the output data of said second multiplication unit, and the output data of said third stage delay circuit;

a second adder for adding the output data of said second multiplication unit, the output data of said third

multiplication unit, and the output data of said first stage delay circuit; and

a switching circuit for selectively switching between the output data of said first adder and the output data of said second adder.

7. The data interpolating device according to claim 3, a plurality of over-sampling circuits are cascade connected, when one set of over-sampling circuit comprises said three stages of delay circuits and said multiplication/addition circuit.

8. A data interpolating device, comprising:

plural stages of delay circuits for successively delaying discrete data sequentially inputted;

a multiplication/addition circuit that performs weighted addition of data outputted from the output stages of said plural stages of delay circuits according to the value of a digital basic function and thereby determines interpolation data for said discrete data sequentially inputted; and

an averaging circuit for calculating the average data of adjacent interpolation data output from said multiplication/addition circuit.

9. The data interpolating device according to claim 8, a plurality of over-sampling circuits are cascade connected, when one set of over-sampling circuit comprises

said plural stages of delay circuits, said multiplication/addition circuit and said averaging circuit.

10. A data interpolating device, comprising:

four stages of delay circuits for successively delaying discrete data sequentially inputted; and

a multiplication/addition circuit that performs weighted addition of data outputted from the output stages of said four stages of delay circuits according to the value of a digital basic function and thereby determines interpolation data for said discrete data sequentially inputted.

11. The data interpolating device according to claim 10, said multiplication/addition circuit comprising:

a first multiplication unit for multiplying the output data of the first stage delay circuit by -1;

a second multiplication unit for multiplying the output data of the second stage delay circuit by 9;

a third multiplication unit for multiplying the output data of the third stage delay circuit by 9;

a fourth multiplication unit for multiplying the output data of the fourth stage delay circuit by -1;

an adder for adding the output data of said first to fourth multiplication units; and

a switching circuit for selectively switching between the output data of said adder and the discrete data input into said first stage delay circuit.

12. The data interpolating device according to claim 10, said multiplication/addition circuit comprising:

a first adder for adding the output data of the first stage delay circuit and the output data of the fourth stage delay circuit;

a second adder for adding the output data of the second stage delay circuit and the output data of the third stage delay circuit;

a first multiplication unit for multiplying the output data of said first adder by -1;

a second multiplication unit for multiplying the output data of said second adder by 9;

a third adder for adding the output data of said first adder and the output data of said second adder; and

a switching circuit for selectively switching between the output data of said third adder and the discrete data input into said first stage delay circuit.

13. The data interpolating device according to claim 10, a plurality of over-sampling circuits are cascade connected, when one set of over-sampling circuit comprises said four stages of delay circuits and said multiplication/addition circuit.

14. A data interpolating device, comprising:

five stages of delay circuits for successively delaying discrete data sequentially inputted; and

a multiplication/addition circuit that performs weighted addition of data outputted from the output stages of said five stages of delay circuits according to the value of a digital basic function and thereby determines interpolation data for said discrete data sequentially inputted.

15. The data interpolating device according to claim 14, said multiplication/addition circuit comprising:

a first multiplication/addition circuit composed of a first multiplication unit for multiplying the output data of the first stage delay circuit by -1, a second multiplication unit for multiplying the output data of the second stage delay circuit by 9, a third multiplication unit for multiplying the output data of the third stage delay circuit by 25, a fourth multiplication unit for multiplying the output data of the fourth stage delay circuit by -1, and an adder for adding the output data of said first to fourth multiplication units;

a second multiplication/addition circuit composed of a fifth multiplication unit for multiplying the output data of said second stage delay circuit by -1, a sixth multiplication unit for multiplying the output data of said fourth stage delay circuit by 9, a seventh multiplication unit for multiplying the output data of said fifth multiplication unit by -1, and an adder for adding the output data of said third multiplication

unit and the output data of said fifth to seventh multiplication units; and

a switching circuit for selectively switching between the output data of said first multiplication/addition unit and the output data of said second multiplication/addition unit.

16. The data interpolating device according to claim 14, a plurality of over-sampling circuits are cascade connected, when one set of over-sampling circuit comprises said five stages of delay circuits and said multiplication/addition circuit.

17. A data interpolating device, comprising:

data acquisition means for acquiring discrete data at a sampling point of notice and discrete data at neighboring sampling points around said sampling point of notice when the discrete data are sequentially inputted; and

interpolation means that performs weighted addition of discrete data acquired by said data acquisition means according to the value of a digital basic function and thereby determines interpolation data for said discrete data at said sampling point of notice successively.

18. The data interpolating device according to claim 17, the operation of said data acquisition means and said interpolation means is repeated multiple times by setting the

output data of said interpolation means as the input of said data acquisition means.

19. The data interpolating device according to claim 17, further comprising:

averaging means for performing an averaging operation of adjacent interpolation data for the interpolation data determined by said interpolation means.

20. A data interpolating method, comprising:

performing weighted addition of discrete data at a sampling point of notice and discrete data at surrounding sampling points around said sampling point of notice according to the value of a digital basic function and thereby determining interpolation data for said discrete data at said sampling point of notice, when the discrete data are sequentially inputted.

21. The data interpolating method according to claim 20, comprising:

replacing discrete data sequentially inputted with two interpolation data determined by performing weighted addition of said discrete data according to the value of said digital basic function.

22. The data interpolating method according to claim 21, further comprising:

performing an averaging operation of adjacent interpolation data for said interpolation data determined by performing weighted addition of said discrete data according to the value of said digital basic function.

23. The data interpolating method according to claim 20, further comprising:

performing weighted addition of interpolation data at a sampling point of notice and interpolation data at surrounding sampling points around said sampling point of notice according to the value of said digital basic function, when the interpolation data are determined by performing weighted addition of discrete data according to the value of said digital basic function, and thereby further determining interpolation data for said interpolation data at said sampling point of notice.

24. A data interpolating method, comprising:

performing weighted addition of discrete data at a sampling point of notice and discrete data at its adjacent sampling points according to the value of a digital basic function when the discrete data are sequentially inputted and thereby successively determining interpolation data at two sampling points from the discrete data at said one sampling point.

25. The data interpolating method according to claim 24, further comprising:

performing an averaging operation of adjacent interpolation data for said determined interpolation data.

26. A data interpolating method, comprising:

performing weighted addition of discrete data at two adjacent sampling points of notice and discrete data at the directly neighboring sampling points of said two sampling points according to the value of a digital basic function when the discrete data are sequentially inputted and thereby successively determining interpolation data interpolating between said two sampling points.

27. A sampling function generating device, comprising:

plural stages of delay circuits for successively delaying singly inputted digital data;

a multiplication/addition circuit that performs weighted addition of data outputted from the output stages of said plural stages of delay circuits according to the value of a digital basic function and thereby determines interpolation data for said singly inputted digital data; and

a plurality of over-sampling circuits that are cascade connected when one set of over-sampling circuit comprises said plural stages of delay circuits and said multiplication/addition circuit.

28. A data interpolation program for enabling a computer to operate as each means according to claim 17.

29. A data interpolation program for enabling a computer to perform a processing procedure of said data interpolation method according to claim 20.

30. A data interpolation program for enabling a computer to perform a processing procedure of said data interpolation method according to claim 24.

31. A data interpolation program for enabling a computer to perform a processing procedure of said data interpolation method according to claim 26.

32. A computer readable recorded medium having stored thereon a program for enabling a computer to operate as each means according to claim 17.

33. A computer readable recorded medium having stored thereon a program for enabling a computer to perform a processing procedure of said data interpolation method according to claim 20.

34. A computer readable recorded medium having stored thereon a program for enabling a computer to perform a processing

procedure of said data interpolation method according to claim 24.

35. A computer readable recorded medium having stored thereon a program for enabling a computer to perform a processing procedure of said data interpolation method according to claim 26.